

What is claimed is:

bulk

1. A sense amplifier, comprising:
 - a pair of cross-coupled inverters, wherein each inverter includes:
 - a transistor of a first conductivity type;
 - a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type;
 - a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a gate of a first one of the pair of transistors in each inverter; and
 - a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.
2. The sense amplifier of claim 1, wherein the transistor of a first conductivity type is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the pair of transistors of a second conductivity type are n-channel metal oxide semiconductor (NMOS) transistors.
3. The sense amplifier of claim 1, wherein the drain region for the pair of transistors and the drain region for the transistor of the first conductivity type in one inverter is further coupled to a gate of the transistor of a first conductivity type and to a gate of a second one of the pair of transistors in the other inverter.
4. A sense amplifier, comprising:
 - a pair of cross-coupled inverters, wherein each inverter includes:
 - a p-channel metal oxide semiconductor (PMOS) transistor;
 - and

100-200-300-400-500-600-700-800-900-1000

A2

a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor is coupled to the drain region for the pair of NMOS transistors;

a bit line coupled to each inverter, wherein each bit line couples to a gate for a first one of the pair of NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region for the PMOS and the NMOS transistors.

5. The sense amplifier of claim 4, wherein the drain region for the PMOS and the NMOS transistors in one of the cross-coupled inverters is further coupled to a gate of the PMOS transistor and to a gate of a second one of the pair of NMOS transistors in the other one of the cross-coupled inverters.

6. The sense amplifier of claim 4, wherein the bit line capacitances are removed from the pair of output transmission lines.

7. The sense amplifier of claim 6, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

8. The sense amplifier of claim 4, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

9. The sense amplifier of claim 8, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

10. A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a second transistor and a third transistor of a second conductivity type, wherein the second and third transistors are coupled at a drain region and are coupled at a source region, and wherein the drain region for the second and third transistors are coupled to a drain region of the first transistor;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a gate of the second transistor in each amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the second and the third transistors.

11. The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the second and the third transistors include n-channel metal oxide semiconductor (NMOS) transistors.

12. The latch circuit of claim 11, wherein the drain region for the PMOS and the NMOS transistors in one of the cross-coupled amplifiers is further coupled to a gate of the PMOS transistor and to a gate of a third transistor in the other one of the cross-coupled amplifiers.

13. The latch circuit of claim 10, wherein the pair of input transmission lines are bit lines and wherein the bit line capacitances are removed from the pair of output transmission lines.

14. The latch circuit of claim 13, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

15. The latch circuit of claim 10, wherein the latch circuit is coupled to a power supply voltage of less than 1.0 Volts.

Sub E1

16. The latch circuit of claim 10, wherein the latch circuit is able to output a full output sense voltage in less than 10 nanoseconds (ns).

Sub B4

17. An amplifier circuit, comprising:

- a pair of cross-coupled inverters, wherein each inverter includes:
 - a transistor of a first conductivity type;
 - a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the first transistor of a first conductivity type and the a dual-gated MOSFET are coupled at a drain region;
 - a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a first gate of the dual-gated MOSFET; and
 - a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters.

Sub E1

18. The amplifier circuit of claim 17, wherein the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the a dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors each driven by one of the dual gates.

Sub E1

19. The amplifier circuit of claim 17, wherein the drain region for one of the cross-coupled inverters is further coupled to a gate of the transistor of the first conductivity type and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters.

Sub E1

20. The amplifier circuit of claim 17, wherein the pair of cross-coupled inverters comprise a sense amplifier, and wherein the sense amplifier is included in a memory circuit.

21. The amplifier circuit of claim 20, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

22. The amplifier circuit of claim 21, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

23. A memory circuit, comprising:
a number of memory arrays;
at least one sense amplifier, wherein the sense amplifier includes:
a pair of cross-coupled inverters, wherein each inverter includes:
a p-channel metal oxide semiconductor (PMOS)
transistor; and
a pair of n-channel metal oxide semiconductor
(NMOS) transistors coupled at a drain region and a source
region, and wherein a drain region of the PMOS transistor is
coupled to the drain region for the pair of NMOS transistors;
a complementary pair of bit lines coupling the at least one sense amplifier to
a number of memory cells in the number of memory arrays, and wherein each one of
the complementary pair of bit lines couples to a gate of a first one of the pair of
NMOS transistors in each inverter; and
a pair of output transmission lines, wherein each one of the pair of output
transmission lines is coupled to the drain region of the PMOS transistor and the
drain region for the pair of NMOS transistors in each inverter.

24. The memory circuit of claim 23, wherein the memory circuit includes a folded bit line memory circuit.

25. The memory circuit of claim 23, wherein the drain region for the PMOS and
the NMOS transistors in one of the cross-coupled inverters is further coupled to a

gate of the PMOS transistor and to a gate of a second one of the pair of NMOS transistors in the other one of the cross-coupled inverters.

26. The memory circuit of claim 23, wherein the at least one sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

27. The memory circuit of claim 23, wherein the at least one sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

28. The memory circuit of claim 23, wherein the memory circuit further includes a number of equilibration and a number of isolation transistors coupled to the complementary pair of bit lines.

29. An electronic system, comprising:
a processor;
a memory device; and
a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:
a pair of cross-coupled inverters, wherein each inverter includes:
a p-channel metal oxide semiconductor (PMOS) transistor; and
a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor is coupled to the drain region for the pair of NMOS transistors;
a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to a

gate of a first one of the pair of NMOS transistors in each inverter;
and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the pair of NMOS transistors in each inverter.

30. The electronic system of claim 29, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volt.

31. The electronic system of claim 29, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

32. An integrated circuit, comprising:
a processor;
a memory operatively coupled to the processor; and
wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:
a pair of cross-coupled inverters, wherein each inverter includes:
a transistor of a first conductivity type;
a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type;
a pair of bit lines, wherein each one of the pair of bit lines is coupled to a gate of a first one of the pair of transistors in each inverter; and
a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

33. A method for forming a current sense amplifier, comprising:
cross coupling a pair of inverters, wherein each inverter includes:
a transistor of a first conductivity type;
a pair of transistors of a second conductivity type coupled at a drain
region and coupled at a source region, and wherein the drain region for the
pair of transistors is coupled to a drain region of the transistor of the first
conductivity type; and
wherein cross coupling the pair of inverters includes coupling the drain
region for the transistor of the first conductivity type and the drain region for the
pair of transistors in one inverter to a gate of the transistor of a first conductivity
type and to a gate of a first one of the pair of transistors in the other inverter.

34. The method of claim 33, wherein cross coupling the pair of inverters
includes forming the first transistor of the first conductivity type as a p-channel
metal oxide semiconductor (PMOS) transistor, and forming the pair of transistors of
a second conductivity type as n-channel metal oxide semiconductor (NMOS)
transistors.

35. The method of claim 33, wherein the method further includes coupling a bit
line to a gate of a second one of the pair of transistors in each inverter.

36. The method of claim 33, wherein the method further includes coupling an
output transmission line to the drain region for the pair of transistors and the drain
region of the transistor of the first conductivity type in each inverter.

37. A method for forming a sense amplifier, comprising:
forming and cross coupling a pair of inverters, wherein forming and cross
coupling each inverter includes:
forming a first transistor of a first conductivity type;

forming a second transistor and a third transistor of a second conductivity type, wherein forming the second and the third transistors includes coupling a drain region and a source region for the second and third transistors, and coupling the drain region for the second and third transistors to a drain region of the first transistor; coupling a bit line to a gate of the second transistor in each inverter; and coupling an output transmission line to the drain region of the first transistor and to the drain region of the second and the third transistors in each inverter.

38. The method of claim 37, wherein forming the first transistor of a first conductivity type includes forming a p-channel metal oxide semiconductor (PMOS) transistor, and wherein forming the second and third transistors of a second conductivity type includes forming n-channel metal oxide semiconductor (NMOS) transistors.

39. The method of claim 37, wherein cross coupling the pair of inverters includes coupling the drain region for second and third transistors and the drain region for the first transistor of the first conductivity type in one inverter to a gate of the first transistor of a first conductivity type and to a gate of a third transistor in the other inverter.

40. A method for operating a sense amplifier, comprising:
equilibrating a first and second bit line, wherein the first bit line is coupled to a gate of a first NMOS transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a gate of a first NMOS transistor in a second inverter in the sense amplifier;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter to a gate of a PMOS transistor and to a gate of a second NMOS transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a gate of a second NMOS transistor in the first inverter.

Sub E7

Sub P1

Sub P2

Sub P3

Sub P4

Sub P5

Sub P6

Sub P7

Sub P8

Sub P9

Sub P10

Sub P11

Sub P12

Sub P13

Sub P14

Sub P15

Sub P16

Sub P17

Sub P18

Sub P19

Sub P20

Sub P21

Sub P22

Sub P23

Sub P24

Sub P25

Sub P26

Sub P27

Sub P28

Sub P29

Sub P30

Sub P31

Sub P32

Sub P33

Sub P34

Sub P35

Sub P36

Sub P37

Sub P38

Sub P39

Sub P40

Sub P41

Sub P42

Sub P43

Sub P44

Sub P45

Sub P46

Sub P47

Sub P48

Sub P49

Sub P50

Sub P51

Sub P52

Sub P53

Sub P54

Sub P55

Sub P56

Sub P57

Sub P58

Sub P59

Sub P60

Sub P61

Sub P62

Sub P63

Sub P64

Sub P65

Sub P66

Sub P67

Sub P68

Sub P69

Sub P70

Sub P71

Sub P72

Sub P73

Sub P74

Sub P75

Sub P76

Sub P77

Sub P78

Sub P79

Sub P80

Sub P81

Sub P82

Sub P83

Sub P84

Sub P85

Sub P86

Sub P87

Sub P88

Sub P89

Sub P90

Sub P91

Sub P92

Sub P93

Sub P94

Sub P95

Sub P96

Sub P97

Sub P98

Sub P99

Sub P100

Sub P101

Sub P102

Sub P103

Sub P104

Sub P105

Sub P106

Sub P107

Sub P108

Sub P109

Sub P110

Sub P111

Sub P112

Sub P113

Sub P114

Sub P115

Sub P116

Sub P117

Sub P118

Sub P119

Sub P120

Sub P121

Sub P122

Sub P123

Sub P124

Sub P125

Sub P126

Sub P127

Sub P128

Sub P129

Sub P130

Sub P131

Sub P132

Sub P133

Sub P134

Sub P135

Sub P136

Sub P137

Sub P138

Sub P139

Sub P140

Sub P141

Sub P142

Sub P143

Sub P144

Sub P145

Sub P146

Sub P147

Sub P148

Sub P149

Sub P150

Sub P151

Sub P152

Sub P153

Sub P154

Sub P155

Sub P156

Sub P157

Sub P158

Sub P159

Sub P160

Sub P161

Sub P162

Sub P163

Sub P164

Sub P165

Sub P166

Sub P167

Sub P168

Sub P169

Sub P170

Sub P171

Sub P172

Sub P173

Sub P174

Sub P175

Sub P176

Sub P177

Sub P178

Sub P179

Sub P180

Sub P181

Sub P182

Sub P183

Sub P184

Sub P185

Sub P186

Sub P187

Sub P188

Sub P189

Sub P190

Sub P191

Sub P192

Sub P193

Sub P194

Sub P195

Sub P196

Sub P197

Sub P198

Sub P199

Sub P200

Sub P201

Sub P202

Sub P203

Sub P204

Sub P205

Sub P206

Sub P207

Sub P208

Sub P209

Sub P210

Sub P211

Sub P212

Sub P213

Sub P214

Sub P215

Sub P216

Sub P217

Sub P218

Sub P219

Sub P220

Sub P221

Sub P222

Sub P223

Sub P224

Sub P225

Sub P226

Sub P227

Sub P228

Sub P229

Sub P230

Sub P231

Sub P232

Sub P233

Sub P234

Sub P235

Sub P236

Sub P237

Sub P238

Sub P239

Sub P240

Sub P241

Sub P242

Sub P243

Sub P244

Sub P245

Sub P246

Sub P247

Sub P248

Sub P249

Sub P250

Sub P251

Sub P252

Sub P253

Sub P254

Sub P255

Sub P256

Sub P257

Sub P258

Sub P259

Sub P260

Sub P261

Sub P262

Sub P263

Sub P264

Sub P265

Sub P266

Sub P267

Sub P268

Sub P269

Sub P270

Sub P271

Sub P272

Sub P273

Sub P274

Sub P275

Sub P276

Sub P277

Sub P278

Sub P279

Sub P280

Sub P281

Sub P282

Sub P283

Sub P284

Sub P285

Sub P286

Sub P287

Sub P288

Sub P289

Sub P290

Sub P291

Sub P292

Sub P293

Sub P294

Sub P295

Sub P296

Sub P297

Sub P298

Sub P299

Sub P300

Sub P301

Sub P302

Sub P303

Sub P304

Sub P305

Sub P306

Sub P307

Sub P308

Sub P309

Sub P310

Sub P311

Sub P312

Sub P313

Sub P314

Sub P315

Sub P316

Sub P317

Sub P318

Sub P319

Sub P320

Sub P321

Sub P322

Sub P323

Sub P324

Sub P325

Sub P326

Sub P327

Sub P328

Sub P329

Sub P330

Sub P331

Sub P332

Sub P333

Sub P334

Sub P335

Sub P336

Sub P337

Sub P338

Sub P339

Sub P340

Sub P341

Sub P342

Sub P343

Sub P344

Sub P345

Sub P346

Sub P347

Sub P348

Sub P349

Sub P350

Sub P351

Sub P352

Sub P353

Sub P354

Sub P355

Sub P356

Sub P357

Sub P358

Sub P359

Sub P360

Sub P361

Sub P362

Sub P363

Sub P364

Sub P365

Sub P366

Sub P367

Sub P368

Sub P369

Sub P370

Sub P371

Sub P372

Sub P373

Sub P374

Sub P375

Sub P376

Sub P377

Sub P378

Sub P379

Sub P380

Sub P381

Sub P382

Sub P383

Sub P384

Sub P385

Sub P386

Sub P387

Sub P388

Sub P389

Sub P390

Sub P391

Sub P392

Sub P393

Sub P394

Sub P395

Sub P396

Sub P397

Sub P398

Sub P399

Sub P400

Sub P401

Sub P402

Sub P403

Sub P404

Sub P405

Sub P406

Sub P407

Sub P408

Sub P409

Sub P410

Sub P411

Sub P412

Sub P413

Sub P414

Sub P415

Sub P416

Sub P417

Sub P418

Sub P419

Sub P420

Sub P421

Sub P422

Sub P423

Sub P424

Sub P425

Sub P426

Sub P427

Sub P428

Sub P429

Sub P430

Sub P431

Sub P432

Sub P433

Sub P434

Sub P435

Sub P436

Sub P437

Sub P438

Sub P439

Sub P440

Sub P441

Sub P442

Sub P443

Sub P444

Sub P445

Sub P446

Sub P447

Sub P448

Sub P449

Sub P450

Sub P451

Sub P452

Sub P453

Sub P454

Sub P455

Sub P456

Sub P457

Sub P458

Sub P459

Sub P460

Sub P461

Sub P462

Sub P463

Sub P464

Sub P465

Sub P466

Sub P467

Sub P468

Sub P469

Sub P470

Sub P471

Sub P472

Sub P473

Sub P474

Sub P475

Sub P476

Sub P477

Sub P478

Sub P479

Sub P480

Sub P481

Sub P482

Sub P483

Sub P484

Sub P485

Sub P486

Sub P487

Sub P488

Sub P489

Sub P490

Sub P491

Sub P492

Sub P493

Sub P494

Sub P495

Sub P496

Sub P497

Sub P498

Sub P499

Sub P500

Sub P501

Sub P502

Sub P503

Sub P504

Sub P505

Sub P506

Sub P507

Sub P508

Sub P509

Sub P510

Sub P511

Sub P512

Sub P513

Sub P514

Sub P515

Sub P516

Sub P517

Sub P518

Sub P519

Sub P520

Sub P521

Sub P522

Sub P523

Sub P524

Sub P525

Sub P526

Sub P527

Sub P528

Sub P529

Sub P530

Sub P531

Sub P532

Sub P533

Sub P534

Sub P535

Sub P536

Sub P537

Sub P538

Sub P539

Sub P540

Sub P541

Sub P542

Sub P543

Sub P544

Sub P545

Sub P546

Sub P547

Sub P548

Sub P549

Sub P550

Sub P551

Sub P552

Sub P553

Sub P554

Sub P555

Sub P556

Sub P557

Sub P558

Sub P559

Sub P560

Sub P561

Sub P562

Sub P563

Sub P564

Sub P565

Sub P566

Sub P567

Sub P568

Sub P569

Sub P570

Sub P571

Sub P572

Sub P573

Sub P574

Sub P575

Sub P576

Sub P577

Sub P578

Sub P579

Sub P580

Sub P581

Sub P582

Sub P583

Sub P584

Sub P585

Sub P586

Sub P587

Sub P588

Sub P589

Sub P590

Sub P591

Sub P592

Sub P593

Sub P594

Sub P595

Sub P596

Sub P597

Sub P598

Sub P599

Sub P600

Sub P601

Sub P602

Sub P603

Sub P604

Sub P605

Sub P606

Sub P607

Sub P608

Sub P609

Sub P610

Sub P611

Sub P612

Sub P613

Sub P614

Sub P615

Sub P616

Sub P617

Sub P618

Sub P619

Sub P620

Sub P621

Sub P622

Sub P623

Sub P624

Sub P625

Sub P626

Sub P627

Sub P628

Sub P629

Sub P630

Sub P631

Sub P632

Sub P633

Sub P634

Sub P635

Sub P636

Sub P637

Sub P638

Sub P639

Sub P640

Sub P641

Sub P642

Sub P643

Sub P644

Sub P645

Sub P646

Sub P647

Sub P648

Sub P649

Sub P650

Sub P651

Sub P652

Sub P653

Sub P654

Sub P655

Sub P656

Sub P657

Sub P658

Sub P659

Sub P660

Sub P661

Sub P662

Sub P663

Sub P664

Sub P665

Sub P666

Sub P667

Sub P668

Sub P669

Sub P670

Sub P671

Sub P672

Sub P673

Sub P674

Sub P675

Sub P676

Sub P677

Sub P678

Sub P679

Sub P680

Sub P681

Sub P682

Sub P683

Sub P684

Sub P685

Sub P686

Sub P687

Sub P688

Sub P689

Sub P690

Sub P691

Sub P692

Sub P693

Sub P694

Sub P695

Sub P696

Sub P697

Sub P698

Sub P699

Sub P700

Sub P701

Sub P702

Sub P703

Sub P704

Sub P705

Sub P706

Sub P707

Sub P708

Sub P709

Sub P710

Sub P711

Sub P712

Sub P713

Sub P714

Sub P715

Sub P716

Sub P717

Sub P718

Sub P719

Sub P720

Sub P721

Sub P722

Sub P723

Sub P724

Sub P725

Sub P726

Sub P727

Sub P728

Sub P729

Sub P730

Sub P731

Sub P732

Sub P733

Sub P734

Sub P735

Sub P736

Sub P737

Sub P738

Sub P739

Sub P740

Sub P741

Sub P742

Sub P743

Sub P744

Sub P745

Sub P746

Sub P747

Sub P748

Sub P749

Sub P750

Sub P751

Sub P752

Sub P753

Sub P754

Sub P755

Sub P756

Sub P757

Sub P758

Sub P759

Sub P760

Sub P761

Sub P762

Sub P763

Sub P764

Sub P765

Sub P766

Sub P767

Sub P768

Sub P769

Sub P770

Sub P771

Sub P772

Sub P773

Sub P774

Sub P775

Sub P776

Sub P777

Sub P778

Sub P779

Sub P780

Sub P781

Sub P782

Sub P783

Sub P784

Sub P785

Sub P786

Sub P787

Sub P788

Sub P789

Sub P790

Sub P791

Sub P792

Sub P793

Sub P794

Sub P795

Sub P796

Sub P797

Sub P798

Sub P799

Sub P800

Sub P801

Sub P802

Sub P803

Sub P804

Sub P805

Sub P806

Sub P807

Sub P808

Sub P809

Sub P810

Sub P811

Sub P812

Sub P813

Sub P814</